Please amend the subject application as follows:

IN THE CLAIMS

Please accept amended claims 1, 7, 8 and 10:

1. (Currently amended) A method of forming a semiconductor device comprising:

sequentially forming a supporting layer and a sacrificial layer over a semiconductor substrate;

forming an opening by patterning the sacrificial layer and the supporting layer;

forming a bottom electrode covering the inner wall and the bottom of the opening;

removing the sacrificial layer by a wet etch process; and

forming a dielectric layer and an upper electrode on the bottom electrode and the supporting layer,

wherein the sacrificial layer is formed of a material having a faster wet etch rate than the supporting layer, and the supporting layer comprises a single layer.

2. (Original) The method as claimed in claim 1, further comprising forming a bottom contact plug on the semiconductor substrate before forming the supporting layer, wherein the opening exposes the bottom contact plug and the opening has a wider width than the bottom contact plug.

3. (Original) The method as claimed in claim 1, wherein the supporting layer is formed of a plasma-enhanced tetraethyl orthosilicate (PETEOS) oxide or a high-density plasma (HDP) oxide.

4. (Original) The method as claimed in claim 1, wherein the sacrificial layer is formed of one material selected from a group consisting of a hydrogen silsesquioxane (HSQ) oxide, a borophosphosilicate glass (BPSG) oxide and a phosphosilicate (PSG) oxide.

5. (Original) The method as claimed in claim 1, wherein the wet etch process is performed by using a HF solution.

6. (Original) The method as claimed in claim 1, further comprising:

forming a dielectric layer over an entire surface of the semiconductor substrate comprising the upper electrode;

patterning the dielectric layer to form a contact hole; and

filling the contact hole with a conductive material to form a contact plug.

7. (Currently amended) A method of forming a semiconductor device comprising:

sequentially forming a supporting layer and a sacrificial layer over a semiconductor substrate;

forming an opening by patterning the sacrificial layer and the supporting layer; and

removing the sacrificial layer by a wet etch process, wherein the sacrificial layer is formed of a material that has a faster wet etch rate than the supporting layer, and the supporting layer comprises a single layer.

8. (Currently amended) The method as claimed in claim 7, further comprising:

forming a dielectric layer over ~~a sacrificial~~ the supporting layer;

patterning the dielectric layer and the supporting layer to form a contact hole; and

filling the contact hole with a conductive material to form a contact plug.

9. (Original) The method as claimed in claim 7, wherein the supporting layer includes a plasma-enhanced tetraethyl orthosilicate (PETEOS) oxide or a high-density plasma (HDP) oxide.

10. (Currently amended) The method as claimed in claim 7, wherein the sacrificial layer includes a hydrogen silsesquioxane (HSQ) oxide, a borophosphosilicate glass (BPSG) oxide ~~and~~ or a phosphosilicate (PSG) oxide.

11. (Original) The method as claimed in claim 7, wherein the wet etch process is performed by using a HF solution.